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THESIS

SINGLE-EVENT ANALYSIS OF LT GaAs MESFET INTEGRATED CIRCUITS

by

Richard A. Radice

September, 1997

Thesis Advisor: Todd R. Weatherford

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There is a growing need for the use of electronics in radiation environments such as space. Gallium arsenide (GaAs) semiconductor technology is highly desirable for these applications because it consumes less power at higher speeds than silicon (Si) and shows superior radiation hardness over silicon technologies except for Single-Event-Upset (SEU). This thesis examines GaAs MESFETs fabricated in the Vitesse H-GaAsIII® process utilized in Direct Coupled FET Logic (DCFL) inverters. These simulations are targeted at determining the vulnerability of these devices to SEU. MESFETs fabricated on low-temperature grown GaAs (LT GaAs) epitaxial layers are investigated in addition to the conventional MESFET process using only bulk GaAs. Two-dimensional computer simulations are performed to determine the most effective method to simulate SEU charge collection mechanisms, and how effective the LT GaAs buffer layer is at reducing SEU vulnerability. This thesis is part of a larger project that is attempting to develop a new wafer design that can be inserted into the current Vitesse fabrication process to produce radiation-hardened circuits. Computer simulations are performed using MIXEDMODE®, which is a SPICE simulator for the ATLAS® device simulation software created by SILVACO International Inc.®

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SINGLE-EVENT ANALYSIS OF LT GaAs MESFET INTEGRATED CIRCUITS

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Lieutenant, United States Navy
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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

There is a growing need for the use of electronics in radiation environments such as space. Gallium arsenide (GaAs) semiconductor technology is highly desirable for these applications because it consumes less power at higher speeds than silicon (Si) and shows superior radiation hardness over silicon technologies except for Single-Event-Upset (SEU). This thesis examines GaAs MESFETs fabricated in the Vitesse H-GaAsIII® process utilized in Direct Coupled FET Logic (DCFL) inverters. These simulations are targeted at determining the vulnerability of these devices to SEU. MESFETs fabricated on low-temperature grown GaAs (LT GaAs) epitaxial layers are investigated in addition to the conventional MESFET process using only bulk GaAs. Two-dimensional computer simulations are performed to determine the most effective method to simulate SEU charge collection mechanisms, and how effective the LT GaAs buffer layer is at reducing SEU vulnerability. This thesis is part of a larger project that is attempting to develop a new wafer design that can be inserted into the current Vitesse fabrication process to produce radiation-hardened circuits. Computer simulations are performed using MIXEDMODE®, which is a SPICE simulator for the ATLAS® device simulation software created by SILVACO International Inc.®

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I. INTRODUCTION

A. PURPOSE

This research utilizes two-dimensional (2-D) device simulation software to understand the mechanisms associated with the Single-Event Effect (SEE) sensitivity of Gallium Arsenide (GaAs) Metal Semiconductor Field Effect Transistors (MESFET). Comparisons are made between discrete simulations and those with the MESFETs implementing a Direct-Coupled Field effect transistor Logic (DCFL) inverter circuit. The effect of the intensity of the SEE will be explored to determine the vulnerability of the circuit. MESFETs fabricated on bulk GaAs and GaAs with a buffer layer of Low-Temperature grown GaAs (LT GaAs) and epitaxial GaAs are simulated to determine if there is any improvement in hardening to Single-Event Upsets (SEU).

B. GOALS

There are two major goals for this project. The first is to develop the most realistic 2-D method of simulating SEUs in Vitesse MESFETs using MIXEDMODE®, the SPICE simulator for the ATLAS® device simulation software created by SILVACO International INC. ® The second is to demonstrate the improvement in SEU hardness that the LT GaAs layer provides.

C. SCOPE

This thesis will examine Vitesse MESFETs both with and without an LT GaAs buffer layer. It compares results from SEU of discrete transistors to that of the MESFETs utilized in a DCFL inverter circuit. The intensity of the event will be varied to explore the range of effectiveness of the device.

D. BENEFITS OF STUDY

This project will provide the research group with a method to analyze what is happening both inside the transistor and in a circuit during an SEU. MESFETs that have been previously modeled will be used to determine their reaction to a single event, providing immediate feedback to device designers as to

the effectiveness of their design and will give insight to possible improvements. The research project that this is a part of will provide current commercial fabrication processes a method to produce radiation-hardened Integrated Circuits (IC) by substituting the bulk wafer with an epitaxial LT GaAs wafer.

E. METHODOLOGY

To start this project, it was necessary to obtain Silvaco ATLAS® models of the Vitesse MESFETs. These models were designed, coded and simulated by two other students involved in the project, specifically, Major James Devers, USMC and Lieutenant Douglas Eskins, USN [12]. A standard inverter design was implemented with these models. A DC transfer characteristic was obtained to verify the proper operation of the circuit and its devices. To simulate an SEU, charge is introduced between the gate and drain of the enhancement device in the form of an optical beam. The intensity of this beam was varied to determine the limitations and behavior of the circuit.

II. BACKGROUND

A. GALLIUM ARSENIDE TECHNOLOGY

Digital integrated circuits are being required to operate at increasingly higher speeds. Many of these circuits are being designed and fabricated with gallium arsenide. Gallium arsenide technologies operate at higher speeds because of a higher electron velocity and mobility. They also draw less power at higher speeds than silicon technologies. It is for these reasons that space-based applications, such as satellites, are turning to GaAs to meet their high-speed requirements while on a small power budget. Even though GaAs has superior tolerance to total ionizing radiation and dose rate effects, a major drawback is that GaAs is more susceptible to the single event radiation effects. Two of the devices that are most common to GaAs logic circuits are the MESFET and Schottky-barrier diode (Figure 2.1). This thesis investigates the mechanisms of an SEU for a MESFET fabricated into a DCFL inverter circuit.

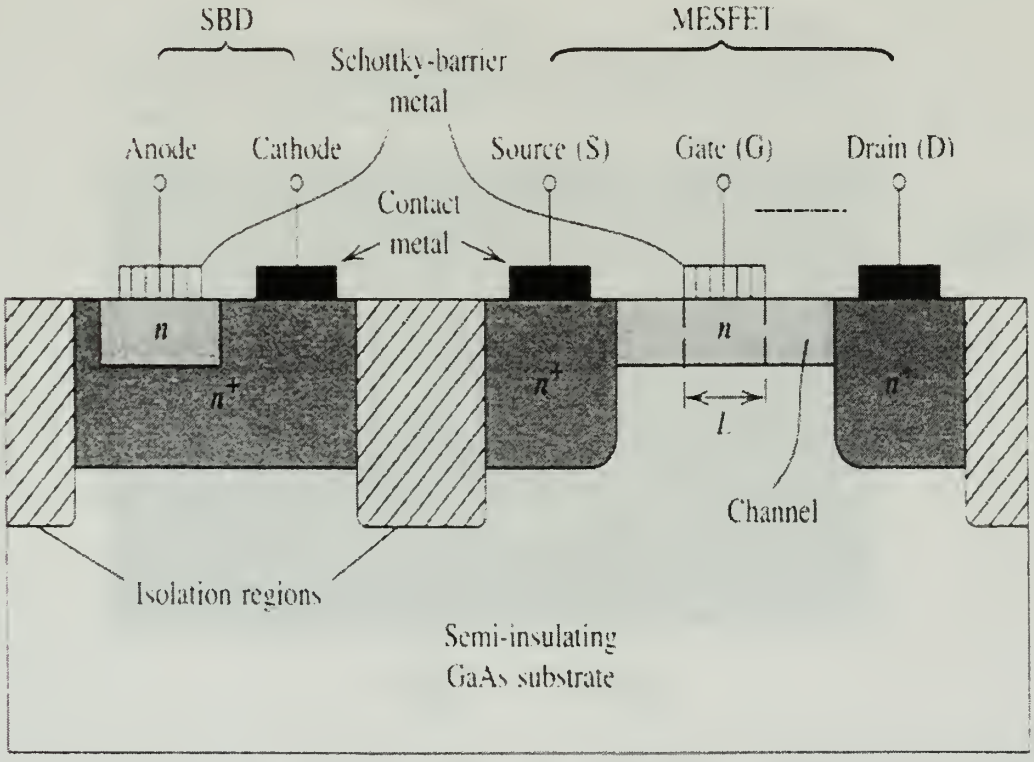

Figure 2.1 Generic representation of the fabrication of GaAs Metal-Semiconductor devices: Schottky-Barrier Diode (SBD) on the left and a MESFET on the right. From [1]

B. VITESSE MESFET

The MESFET models used in the simulations for this thesis model the Vitesse Semiconductor H-GaAs-III® process (Figure 2.2). A MESFET is formed by placing an n-implant on top of a p-implant, then placing the n+ ohmic implants. Metal contacts are placed over each ohmic implant to form the source and the drain. A third, rectifying, contact is centered in the region between the source and the drain to form the gate. The Schottky contact between the metal and the semiconductor form a depletion region below the gate. Applying a potential to the gate will cause the depletion region to change size, determining the size of the conductive channel for current to flow between the drain and the source. There are two types of devices: enhancement and depletion. An enhancement MESFET (EFET) does not conduct at a zero bias between the gate and the source whereas a depletion MESFET (DFET) does. Vitesse manufactures enhancement and depletion mode devices in the H-GaAs-III® process.

Figure 2.2 Cross-section of a Vitesse MESFET with an LT Buffer Layer. The conventional device does not have the LT GaAs Buffer Layer and the AlAs diffusion barriers.

C. INVERTER INTEGRATED CIRCUIT

The inverter simulated for this thesis models a Vitesse DCFL inverter (Figure 2.3). The active device in this circuit is an Enhancement mode MESFET (EFET). The gate of the EFET is being driven by a previous inverter and the source is connected to a common (ground) node. The drain is connected to a two-volt power supply via a depletion-mode MESFET (DFET) and to the output. A Schottky-barrier diode can effectively be used to model the gate-source junction in the next stage of the circuit due to their similarity to the MESFET gate characteristics (Figure 2.1).

An inverter output generates the opposite logic value that is applied to the input. For the Vitesse DCFL modeled, a low logic value, or zero, is approximately zero volts and a high logic value, or one, is approximately 0.58 volts. These values correspond to the on-voltage of the gate junction of the following inverter load.

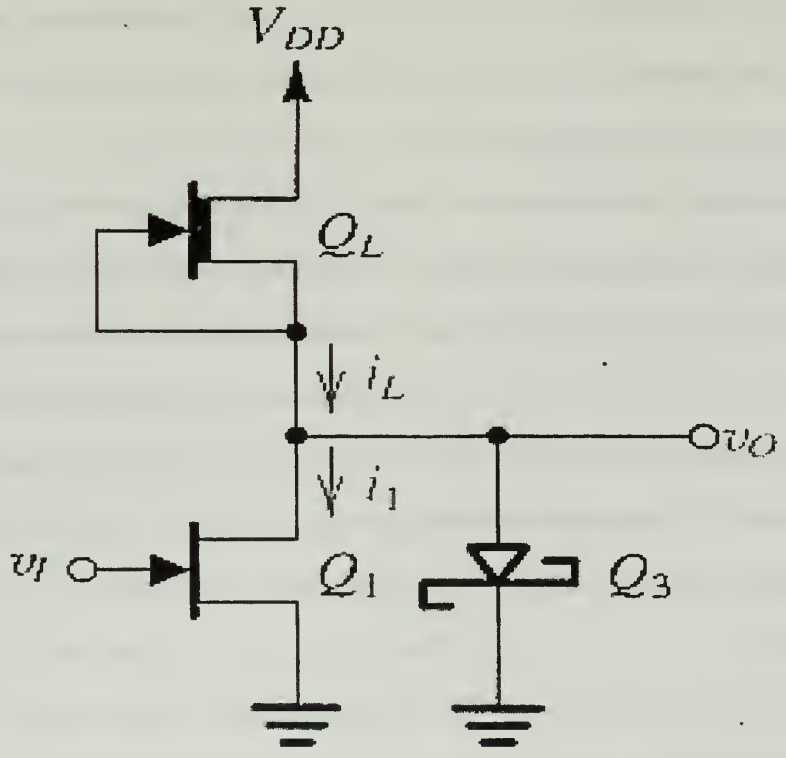

Figure 2.3 Schematic diagram of a GaAs DCFL Inverter. An EFET with DFET active load, driving a SBD that models the gate of the next EFET/DFET inverter. From [1]

When a zero is applied to the input, the EFET does not conduct, thus preventing current flow from the EFET's drain to source. Current flows to the gate of the next EFET. The output (drain) voltage is effectively pulled-up by the power supply via the DFET to the value of next EFET gate-source junction. When the input voltage to the initial inverter is increased above the device threshold, the depletion region is narrowed allowing current flow through the channel between the drain and the source, turning the transistor on. This current flow effectively shorts the output to the source, pulling it down to a common (ground) value.

D. SINGLE EVENT UPSET

Digital integrated circuits fabricated in GaAs have a higher resistance to total dose radiation than silicon, but are more susceptible to single events. [9] A single event is when a high energy particle strikes the circuit inducing ionization. A single event upset (SEU), also called soft-error, occurs when the particle strikes a digital circuit element and causes the output to change from a one to a zero, or from a zero to a one. A transistor that is biased off is most susceptible to SEUs, especially in high electric field areas such as in the drain and gate depletion regions. A strike in this area can introduce enough charge into the device to induce the EFET to conduct, upsetting the output.

This thesis explores the mechanisms at work in the transistor that govern these charge collection effects. There are three distinct periods during an SEU where different charge collection mechanisms are dominant. The first is during and directly following the particle strike, it lasts only a few picoseconds and is dominated by prompt and drift effects. The second period lasts for tens of picoseconds, and is characterized by a parasitic bipolar action between the source n+ and drain regions with excess holes acting as a base. The third is a back-gating effect that lasts until the circuit recovers. These will be examined closely in Chapter IV.

E. LT GaAs

Buffer layers have been proposed to improve the recombination of carriers below the GaAs FET during charge collection events. Low-temperature grown GaAs (LT GaAs), with its three order-of-magnitude shorter carrier lifetime than normally-grown GaAs, was suggested as a candidate to harden GaAs ICs [2]. Charge collection simulations using LT GaAs as a buffer suggest a significant reduction in charge

collection can be attained. Recently, others have investigated the effects of buffer thickness on charge collection [3]. The feasibility of LT GaAs buffers to reduce SEU has been demonstrated in other GaAs FET processes [4,5] but not in a MESFET technology. [6]

Inserting the LT GaAs buffer layer was accomplished by growing Molecular Beam Epitaxy (MBE) GaAs on a bulk GaAs wafer, then lowering the growth temperature to grow non-stoichiometric arsenic-rich GaAs. The low temperature growth is followed by a deposition of high quality epitaxial GaAs above the LT GaAs and an annealing step [7]. The purpose of the arsenic-rich material is to introduce complexes that trap and recombine excess electrons and holes. The effective carrier lifetime of the LT GaAs material is approximately 1-10 picoseconds, several orders of magnitude lower than the bulk GaAs characteristic lifetime of 1 nanosecond [8]. Ionized charge in the buffer layer recombines 2 to 3 orders of magnitude faster than in the substrate or in the upper epitaxial layer. [9]

Implementing LT GaAs buffers in implanted bulk GaAs MESFET processes is challenging because of the manufacturing issues. However, if VLSI circuits can be fabricated in a GaAs MESFET DCFL process on LT GaAs, it should be possible to produce radiation-hardened Application Specific ICs (ASICs) in excess of fifty thousand gates and with clock speeds in excess of 500 MHz by just substituting bulk wafers with epitaxial wafers utilizing LT GaAs buffers into the fabrication process. [6] There would no longer be a need to redesign circuits to make them SEU-hard. There would be a significant savings in time, effort and money because the only modifications would be to the initial semiconductor wafer. The fabrication lines and circuit designs remain unchanged.

Improvement in the SEU performance of devices with the LT GaAs buffer need to be made. Fabricating test circuits for physical testing can be time consuming and expensive. Computer simulation techniques can be used to obtain the types of data that physical testing would generate and also to provide further insight into the mechanisms at work inside the transistor. This is discussed in depth in the next chapter.

III. SIMULATIONS

A. SOFTWARE

The simulations and their graphical analysis were conducted using the Virtual Wafer Fab (VWF) Framework© software by SILVACO International Inc. It is a family of process and device simulation tools that provides users with the ability to perform and graphically analyze large, simulation-based semiconductor designs. It contains three Core Tools that are used to numerically simulate the processing and electrical testing of semiconductor devices, Automation Tools that create a database of results for comparison to experiments and a collection of Interactive Tools that provide the graphical interface for user interaction. Figure 3.1 graphically represents this relationship. [10]

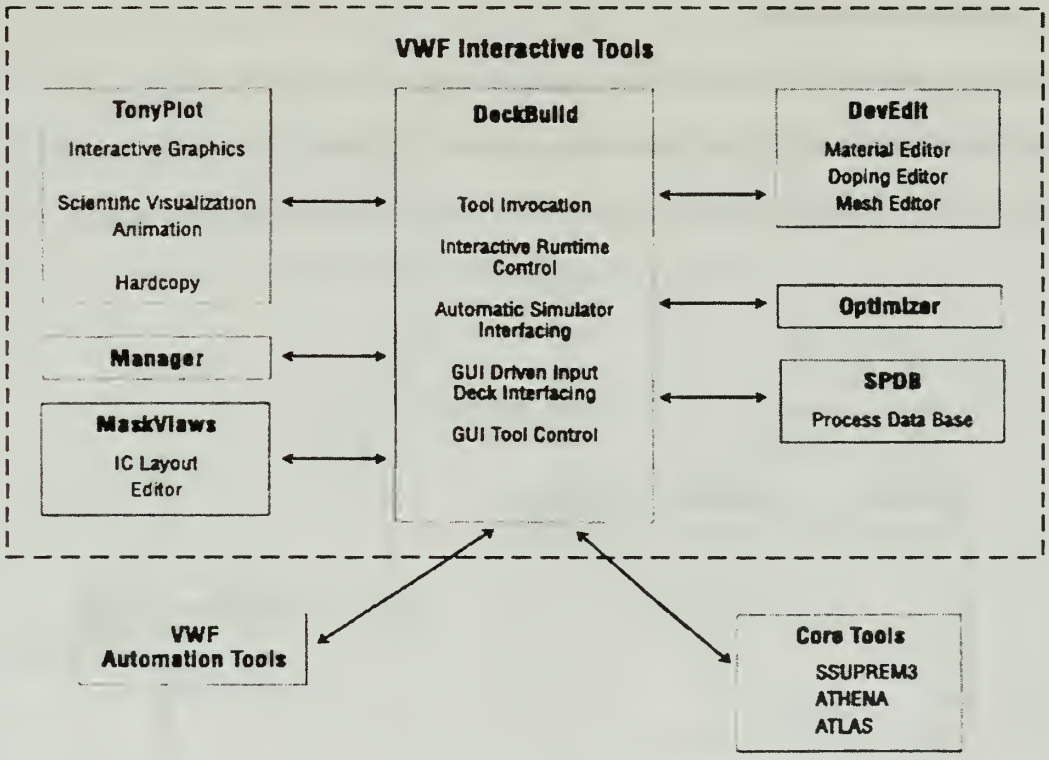

Figure 3.1 Silvaco VWF Framework from Ref. [10]

The simulations for this thesis were conducted using MIXEDMODE©. MIXEDMODE© is the circuit simulator included in the ATLAS© core tool. It allows for the performance of devices created in ATLAS© to be numerically analyzed in a circuit with SPICE circuit models. It exchanges terminal

boundary conditions between the analysis of the SPICE model circuit and ATLAS© device terminals. The graphical analysis for this thesis were conducted using TonyPlot©. TonyPlot© is the graphical post processing tool that is used to visualize results of all Silvaco simulators. It can plot circuit parameters at nodes and in the various branches, as well as specified parameters in a device cross section. There is also an option to take several steps of a simulation and combine them into a movie. [11]

This software has provided invaluable insight into the mechanisms at work inside a circuit component MESFET following a particle-induced SEU. The concentrations of holes and electrons, and their magnitude and direction of flow, could be determined by breaking the event down into time segments and then looking inside the transistor at each time step.

B. DISCRETE CIRCUIT

Previous studies [2-9] were conducted on discrete transistors.(Figure 3.2) None of these simulations used the Silvaco software. Discrete simulations were run in Silvaco to compare to circuit simulations. A constant bias was placed on the drain of an ATLAS MESFET model with the gate

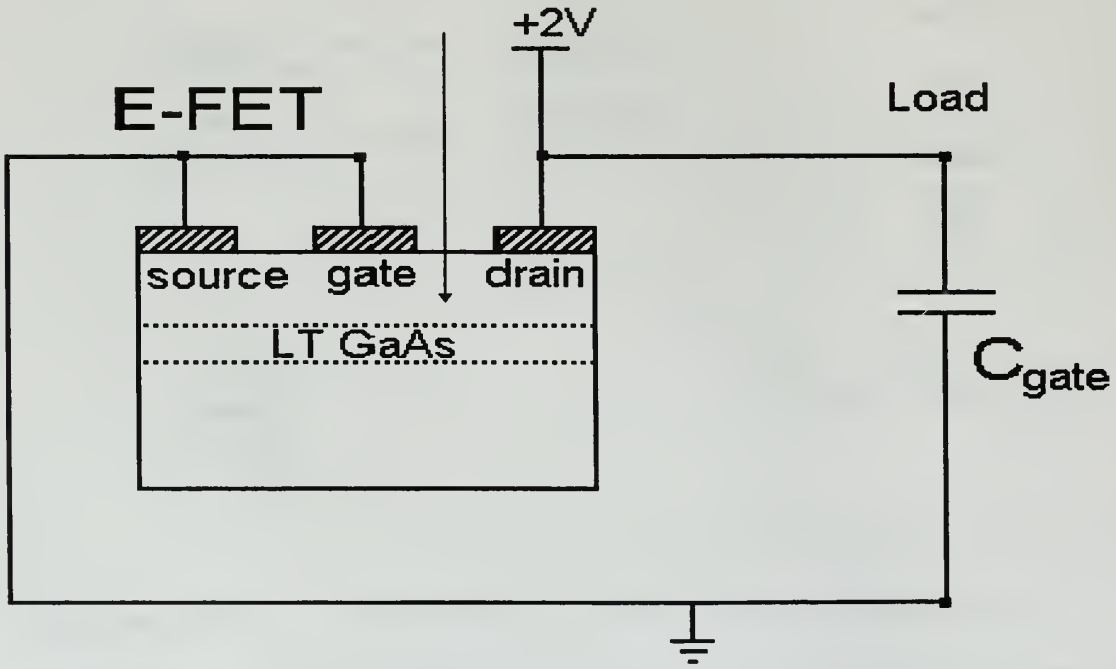

Figure 3.2 Circuit Layout for Discrete Transistor Simulation. The ion strike occurs between the gate and the drain of the MESFET.

and source grounded. A capacitor was placed from drain to ground. The ion strike was centered between gate and drain at a right angle. This setup is depicted in Figure 3.2. Note that no LT GaAs buffer was utilized in the previous analysis.

C. INVERTER CIRCUIT

The inverter circuit (Figure 3.3) is used to determine the performance of the Vitesse MESFET in a circuit during an SEU. This is the first instance of modeling charge collection in an EFET with an active load. In a digital IC, the inverter would be driving the gate of the next inverter. To model this load, a diode and a capacitor were used in the SPICE model. The capacitance could have been specified in the diode model but by modeling the capacitance of the gate and gate-source junction separately, their individual contributions can be analyzed. During identical runs, the DFET was modeled using a SPICE resistor or a SPICE MOSFET setup as a DFET to determine if the circuit reacted different with an active depletion load, vice a passive one. The circuit is biased with two volts at the drain of the DFET and the gate and source are grounded. By modeling a logic zero at the input to this logic gate, the EFET, and therefore the entire gate, is most vulnerable to an event turning the EFET on and upsetting the output.

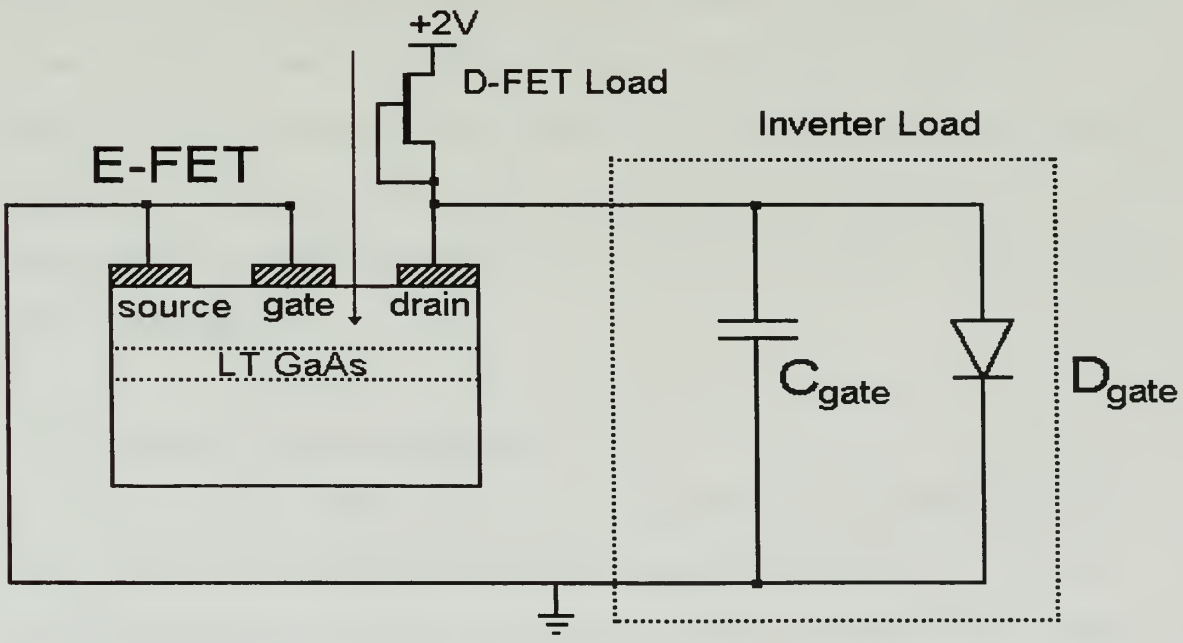

Figure 3.3 Circuit Layout for Inverter Simulation. The ion strike occurs between the gate and the drain of the MESFET.

MIXEDMODE© simulations were performed using conventional device models in both of the above configurations. Devices that included the LT GaAs buffer were also tested in the inverter configuration. The results from these simulations are presented in the next chapter.

IV. RESULTS

A. INVERTER BIAS CONDITIONS

Models of Vitesse EFETs, produced using Silvaco ATLAS software, were provided by Major James Devers, USMC and Lieutenant Douglas Eskins, USN[12]. There is a two-dimensional mesh that defines the location of points in the cross-section of a device where the mathematical evaluation will be performed. The EFET meshes were refined so that there would be a greater number of calculations performed in the area where the single event would be introduced. This refinement not only increases the accuracy of the simulation but can decrease the simulation time. The Silvaco software will automatically decrease the time step when its mathematical algorithms have trouble converging in areas where the mesh is too large for the changes that are occurring. The time step will be halved until a solution is possible. Each iteration takes several hours and no progress on the simulation is made. When the simulation begins progressing with the smaller time steps, it will require more steps until it reaches completion.

Inverters were formed using the refined-mesh EFETs and a SPICE depletion-mode MOSFET as the DFET (Figure 3.3). To obtain a solution for the biased inverter, the power source (V_{dd}) was increased from zero to two volts with solutions performed at each step. The solution following the final step is saved, to be used as the initial conditions for all following simulations. Since there will be several follow-on simulations for each circuit, and each of those must start by solving for the initial conditions of the circuit, providing an initial starting point greatly reduces the simulation time. It is estimated that for a single simulation, between one-hundred twenty-five and one hundred fifty hours of computer simulation time was saved by using this method.

B. INVERTER DC CHARACTERISTICS

To confirm that the designed inverter circuit operates properly, a DC transfer characteristic was obtained. Starting with the biased circuit, the input (gate) voltage was swept from zero to one volt. By measuring the output (drain) the overall DC voltage performance (Figure 4.1) can be evaluated. Inverters using both the standard device and the one fabricated on a LT Buffer were within specifications. When the

input voltage was low, the output was high and when the input became high, the output became low. There is a range of input voltages that will force the inverter output high, and another range of input voltages that will force a low output. Similarly, there is a range of output voltages for which the inverter output will be considered high, and another range of output voltages that will be considered a low output. We use these voltages to calculate the noise margin of the gate. The low noise margin (NM_L) is the difference between the maximum the voltage at the input can be and still be considered low (V_{ILmax}) and the maximum output voltage the will be considered low(V_{OLmax}) (see equation 4.1). The high noise margin (NM_H) is the difference between the minimum the voltage at the output can be and still be considered low (VO_{Hmin}) and the minimum input voltage the will be considered high (V_{IHmin}) (see equation 4.1). These numbers can be obtained graphically from figure 4.1. The noise margins changed by 20 to 30 mV when implanting the LT GaAs buffer. This was due to the different p-profile.

$$NM_L = | V_{ILmax} - V_{OLmax} | \quad (4.1)$$

$$NM_H = | V_{OHmin} - V_{IHmin} | \quad (4.2)$$

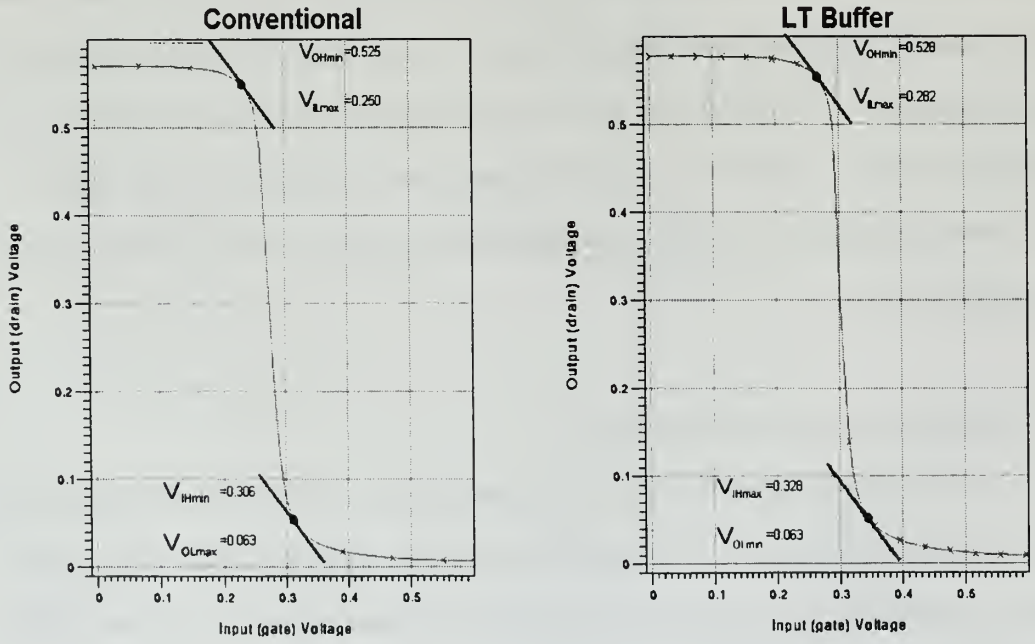

Figure 4.1 Inverter DC transfer characteristics using standard (left) and LT buffered (right) EFETs.

The noise margins for the EFETs are:

$$NM_{Lconventional} = |.250 - .063| = 0.187 Volts$$
$$NM_{Hconventional} = |.525 - .306| = 0.219 Volts$$
$$NM_{Lbuffered} = |.282 - .063| = 0.219 Volts$$
$$NM_{Hbuffered} = |.528 - .328| = 0.200 Volts$$

C. DISCRETE VERSUS CIRCUIT SIMULATIONS

Identical optical pulses were used for the SEU simulation of a conventional EFET in both an inverter circuit and a discrete configuration. The intensity of the pulse was 10 Megawatts/cm^2 (100 Millijoules/um^2). It had a rise and fall time of a quarter of a picosecond and a pulse width of one-half of a picosecond. It is a 0.82 LET MeV/mg/cm^2 event, introducing 47 fC/μm of charge into the device. To analyze the charge that is collected by the device, the drain current will be analyzed (Figure 4.2).

Integrating the drain current shows the charge collected during the simulation, because current is the time rate of change of the charge. The discrete device collected 772 fC, while the inverter collected only 88 fC. Figure 4.2 shows the typical shape to these SEU waveforms. There is an initial, short-duration spike called prompt. It is associated with the event and is mainly due to photo-conductive currents from the pulse and the initial drift of the carriers that are introduced. The second, longer duration hump is due to a parasitic bipolar effect between the excess holes and the two n-wells. It allows current flow in the manner of a bipolar transistor. The third is back-gating that dominates after the bipolar effect has dissipated. It is characterized by charge in the substrate opening the channel between the drain and source as if it were the gate of the transistor.

Comparisons of the inverter to the discrete transistor simulation shows an exaggeration of all the charge collection mechanisms. The prompt in the discrete simulation shows a thirteen percent increase. The bipolar effect is six times as intense, for twice as long. Even the back-gating is more dominant in the discrete case because there in no interaction with other circuit devices. Discrete simulations can be a useful tool to examine charge collection mechanisms in a device but the inaccuracies associated with it make impractical for the prediction of single-event effects in circuits.

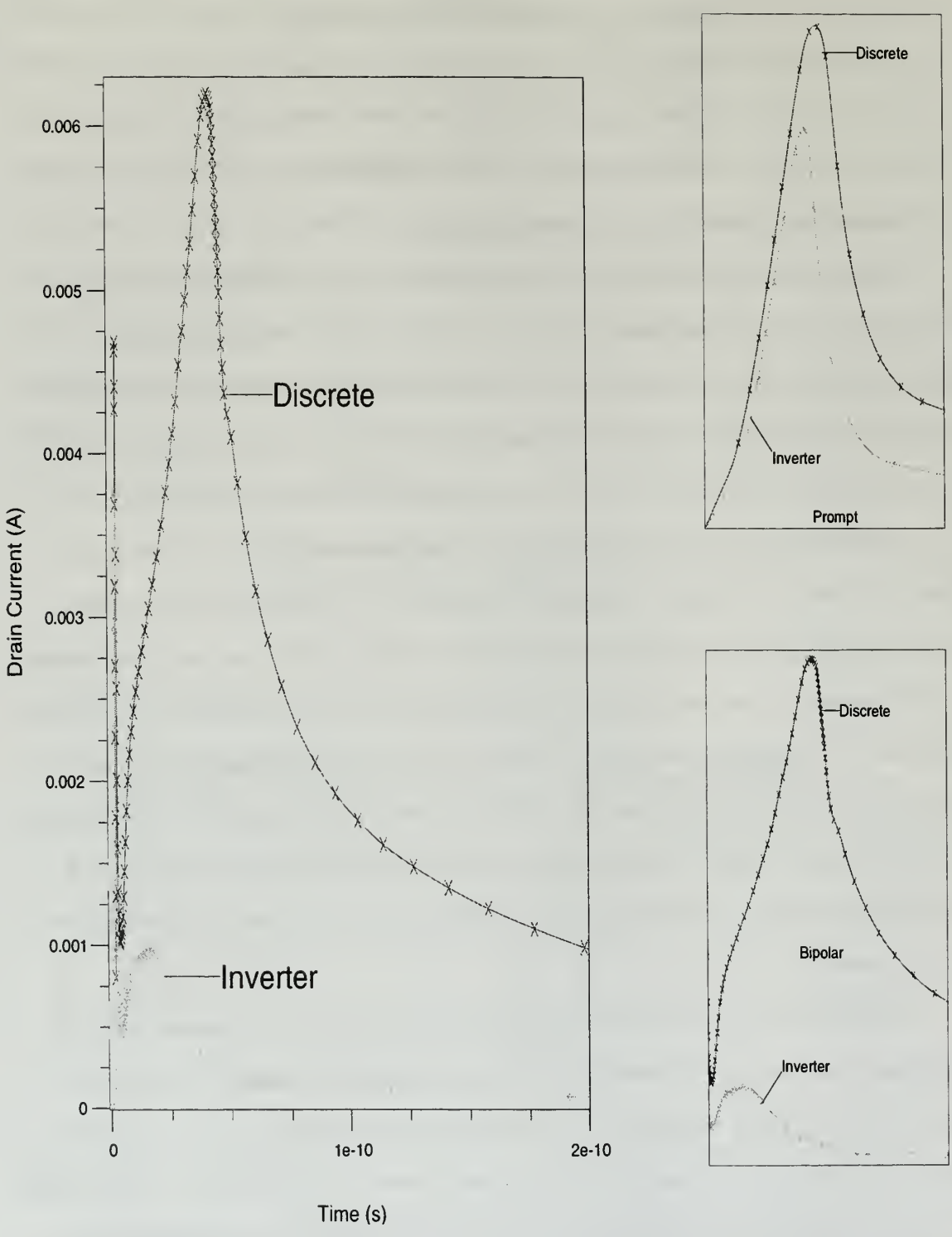

Figure 4.2 EFET drain current of a discrete and inverter SEU simulations. The graph on the left shows the form of the entire event and the smaller graphs give better resolution of the first two peaks. The prompt peak goes from 2 to 3 ps, and the bipolar peak goes from 3 to 30 ps.

D. CHARGE COLLECTION MECHANISMS

Several mechanisms are occurring, as can be observed in the drain-current trace in Figure 4.3. Two peaks can clearly be observed. Figure 4.4 shows the terminal currents of the conventional device. The initial peak in Figure 4.5 shows the gate current (holes) exceeding source current due to a photo-conductive effect at the surface. Because the ionization track has passed through the n+ drain ohmic implant, electron current is at a maximum due to drift. Previous modeling which utilized only uniform-doped regions and different gate-ohmic spacing [3] did not show photo-conductive effects at the surface of the drain ohmic implant. Figure 4.5 is a 2-dimensional plot representing the log scale of electron current minus hole current for the first peak in Figure 4.3. Electrons are removed from the track region and the drain contact due to the high drain potential held by the subsequent inverter gate capacitance.

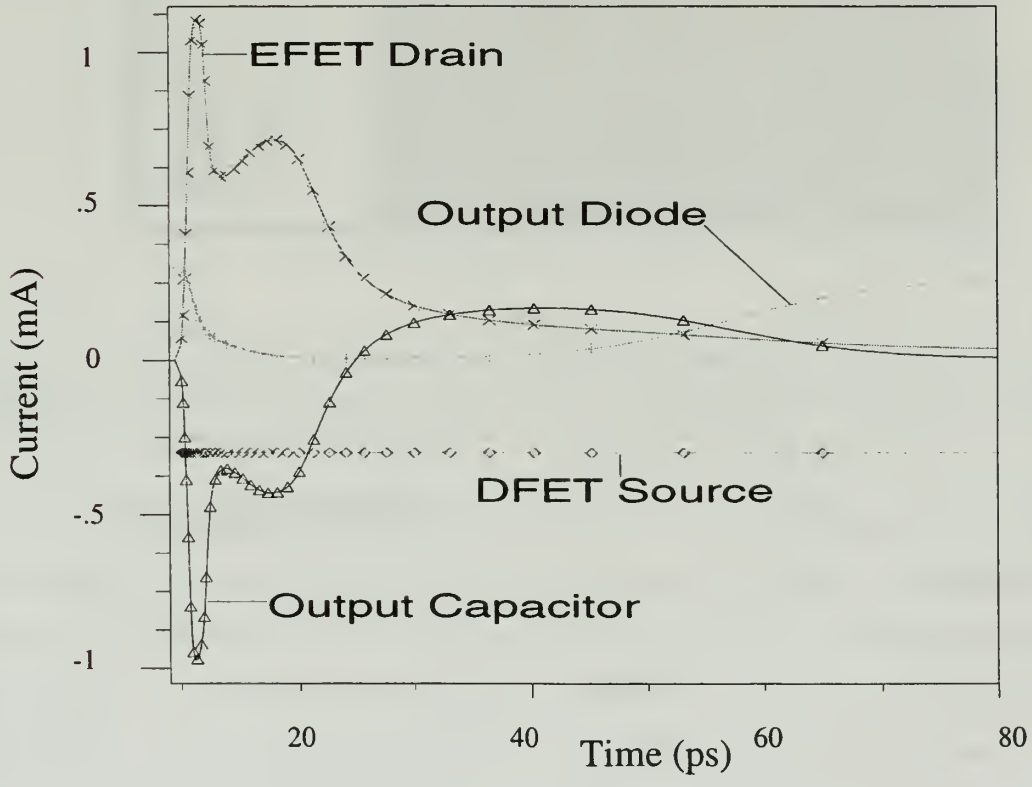

Figure 4.3 . Currents of the E-FET drain, gate diode, capacitor and active load.

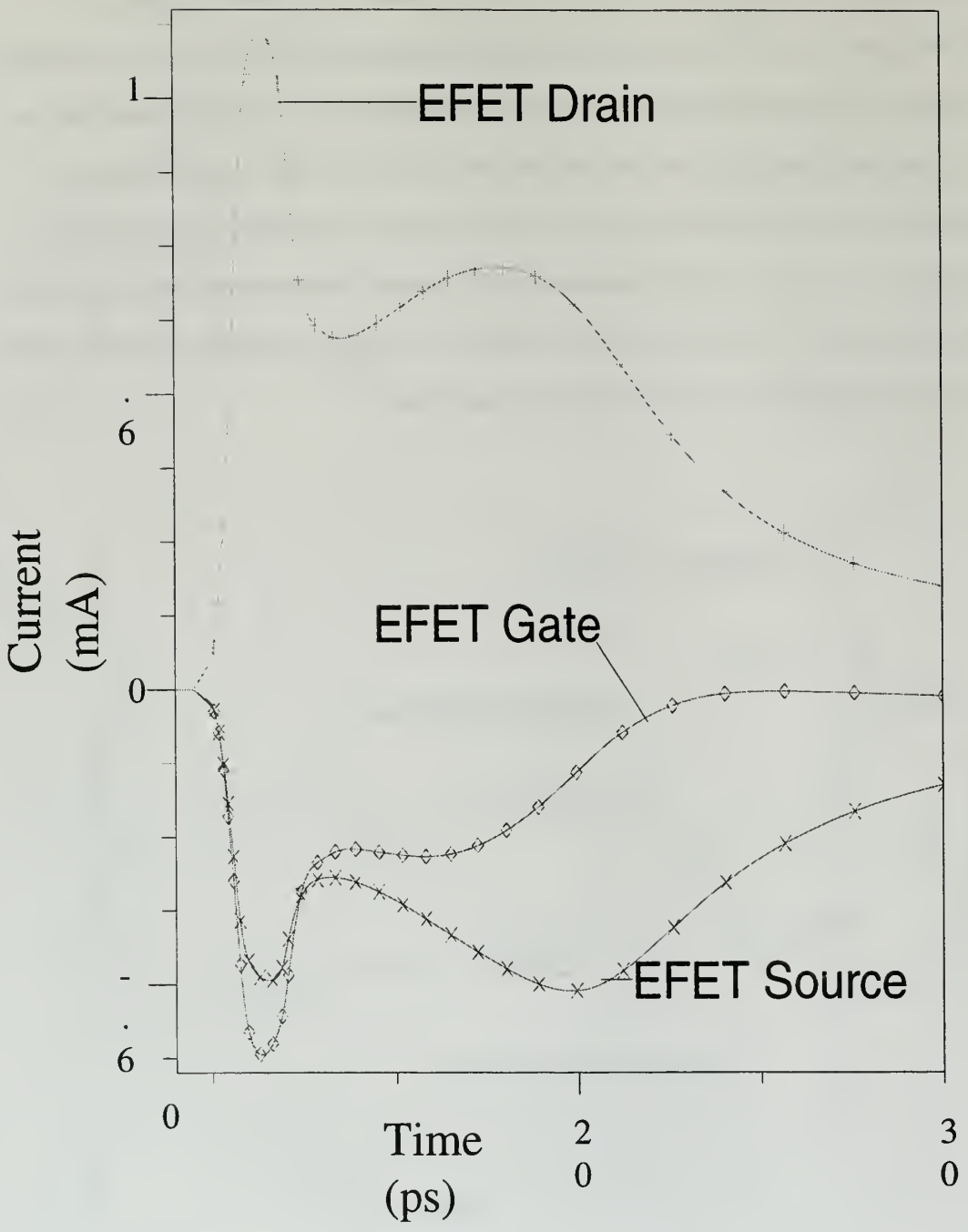

Figure 4.4 Terminal currents of the E-FET.

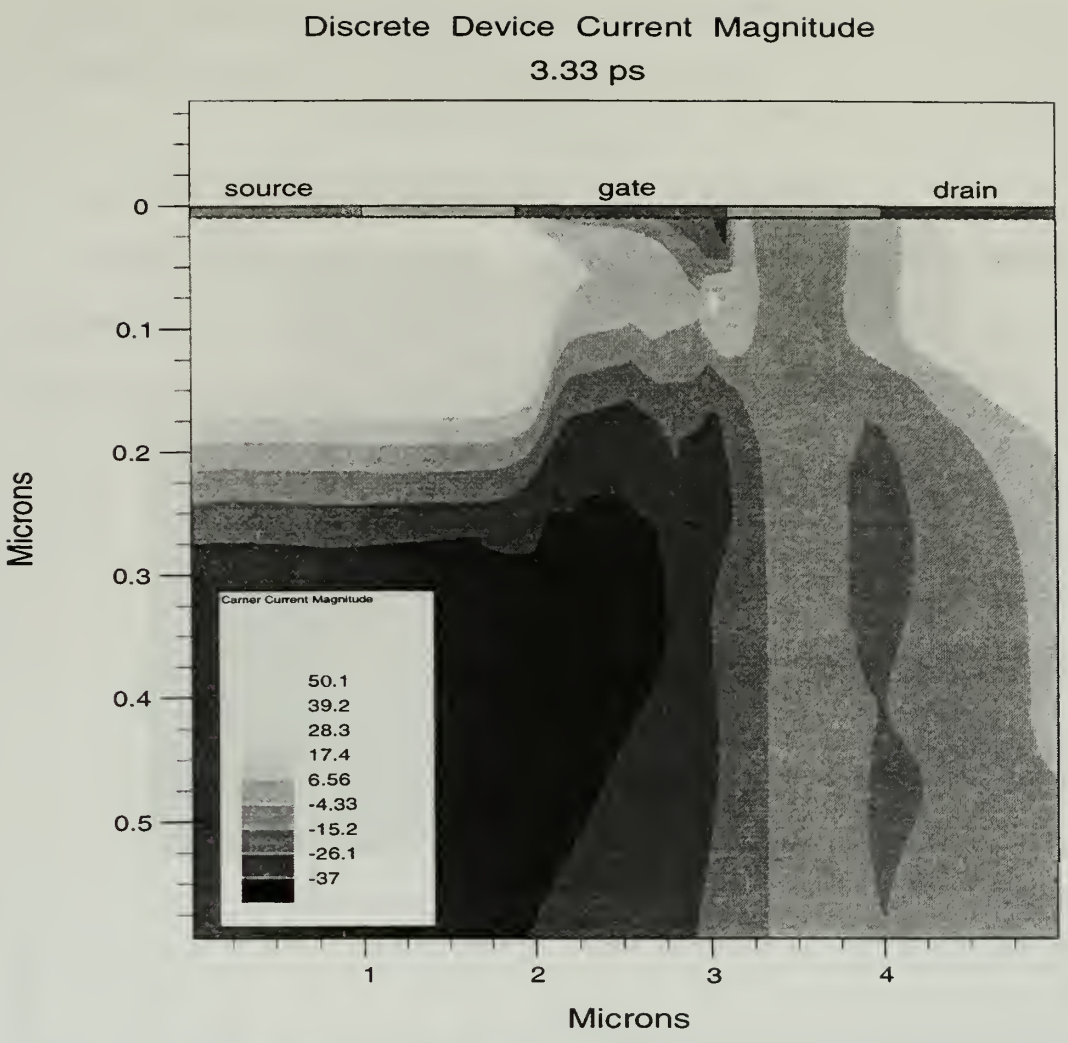

Figure 4.5 Cross-section of the conventional E-FET current densities. Positive values in the plot are regions of high electron current density, negative values are regions of high hole current density. Notice electron current dominates along the surface of the transistor due to photo-conductivity.

Hole current has been observed to come from two sources, the initial particle ionization and the p region beneath the gate. The hole current supplied by this "p-reservoir" below the source implant sets up conditions for a temporary parasitic bipolar action [13]. By the second peak, as shown in Figure 4.6, the hole current supplied from the "reservoir" toward the gate contact acts as a base current to a bipolar NPN. The source and drain implants act as emitter and collector, while excess holes below the channel act as a base. However, the positive potential of the hole "reservoir" competes to backgate the FET channel to provide source electrons to the drain by modulating the bottom of the FET channel. At the source side of the channel region, back channel modulation can be observed while at the same time, hole current below the gate and channel supplies the bipolar mechanism.

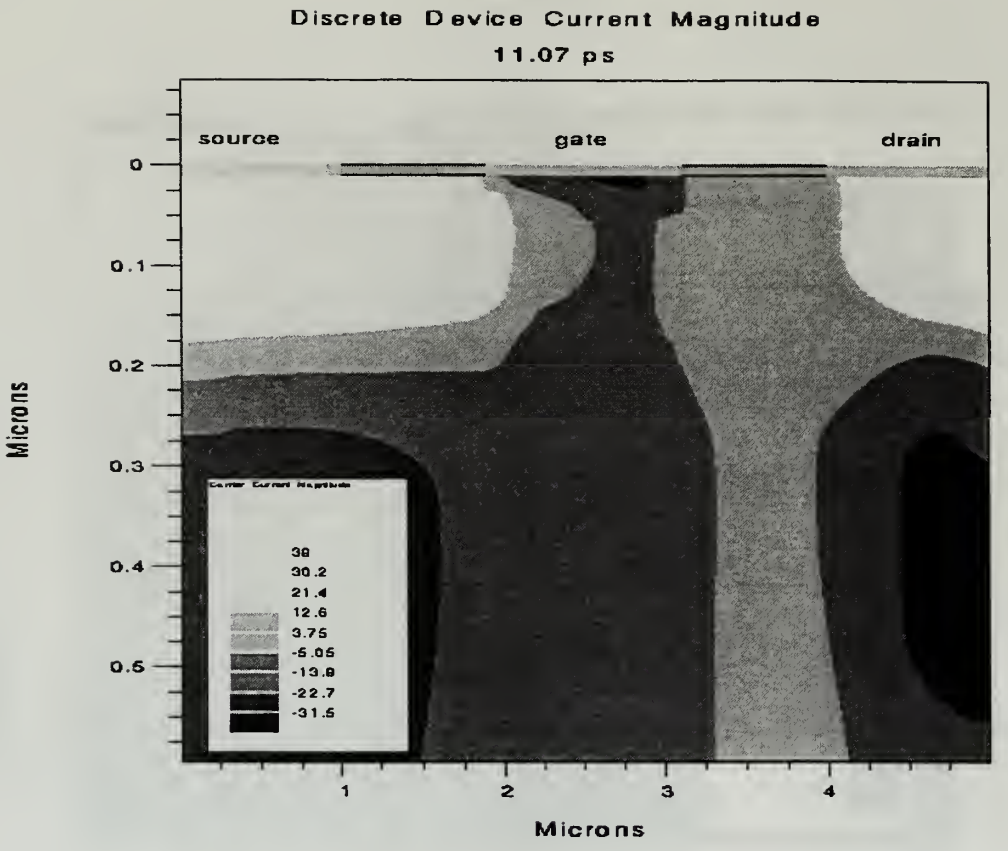

Figure 4.6 Cross section of electron and hole current occurring at the second peak of drain current in Figure 4.3. Notice hole current dominants the region under the gate, supporting a bipolar effect

Based on the 2-D analysis, the bipolar effect should be less severe and backgating mechanism may be much more dominant in a 3-D simulation. In this 2-D simulation, the plane of ionization shields the electrons on the source side. In a 3-D case, shielding by the ionization track would occur only at one location along the FET's gate width. The effect of the "p-reservoir" would be more dominant when compared to the initial prompt drift component in a 3-D simulation.

From these simulations, we observe charge collection from: 1) prompt charge due to ionization in the ohmic implant, 2) photo-conductive collection between drain and gate, 3) hole collection at the gate from the ionization, 4) gate hole collection due to holes below the source, 5) electrons modulated below the

channel, and 6) a source-to-drain bipolar current controlled from holes in (3 and 4). The objective of the LT GaAs buffer is to limit as many of these contributions as possible.

E. LT GaAs BUFFERED VERSUS BULK GaAs SUBSTRATE

Figure 4.7 shows the effect of adding an LT GaAs layer. The reduction in the effects due to the initial prompt (first peak) charge collection can best be seen in the upper right sub-plot. The peak intensity is nearly halved and the amount of charge collected is reduced from 2.5 fC to 1.0 fC.

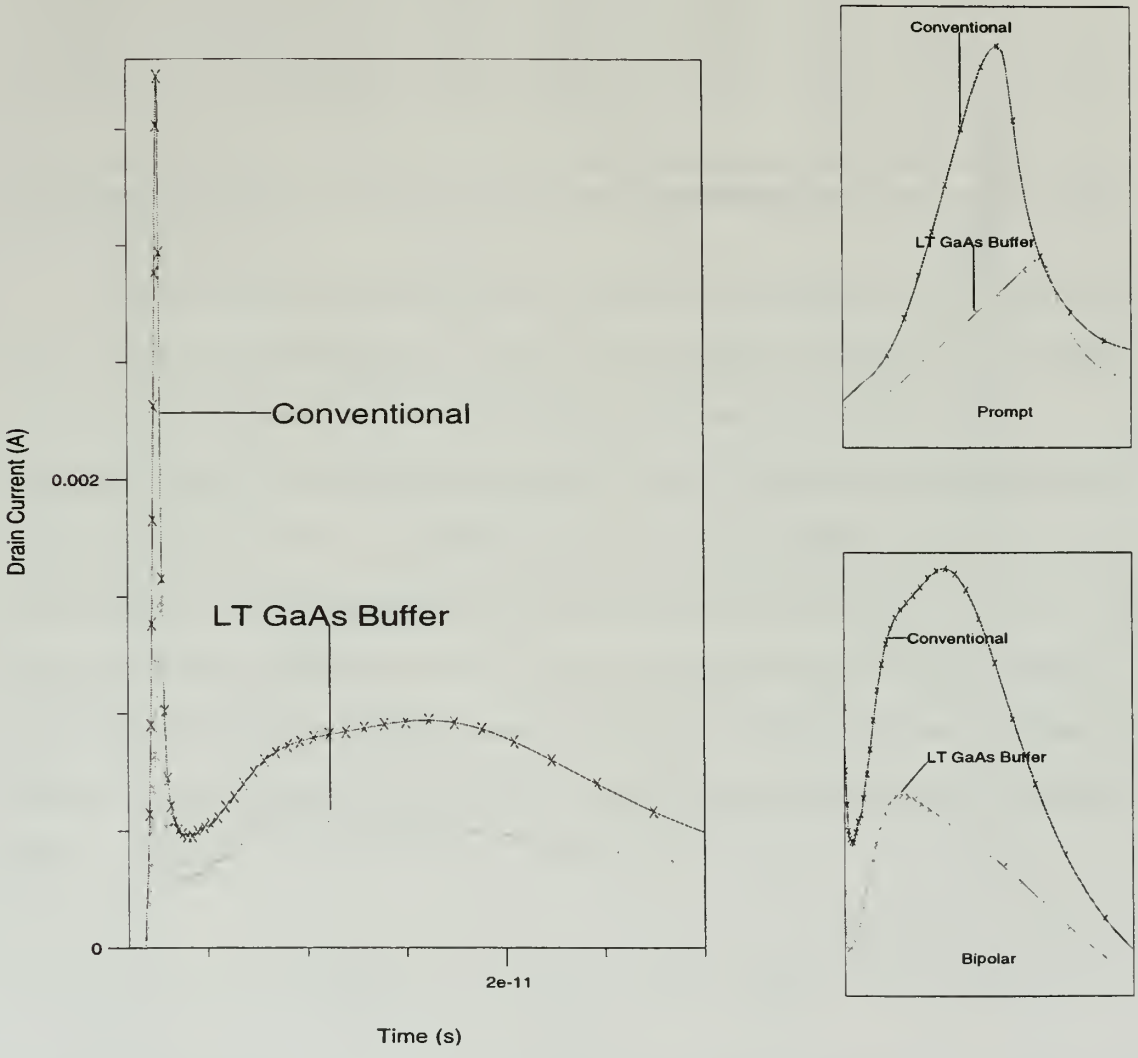

Figure 4.7 EFET drain current of an inverter SEU simulations, one with a conventional EFET and the other with LT GaAs Buffered EFET. The graph on the left shows the form of the entire event and the smaller graphs give better resolution of the first two peaks. The prompt peak goes from 2 to 3 ps, and the bipolar peak goes from 3 to 30 ps.

The lower right sub-plot of Figure 4.7 shows that the parasitic bipolar effect is reduced, collecting 15 fC in the buffered device as opposed to 7.5 fC in the conventional device. Overall, the amount of charge collected was reduced from 72 fC to 34 fC by adding the LT GaAs buffer layer. While the charge collected is responsible for causing the upset, it is the output of the circuit that is ultimately important. Figure 4.8 shows the output voltage for both devices. It is clear that the voltage is not upset as much, or for as long in the device that has an LT GaAs layer. This is a direct result of the charge collected in the device that forces it to conduct while it is biased off.

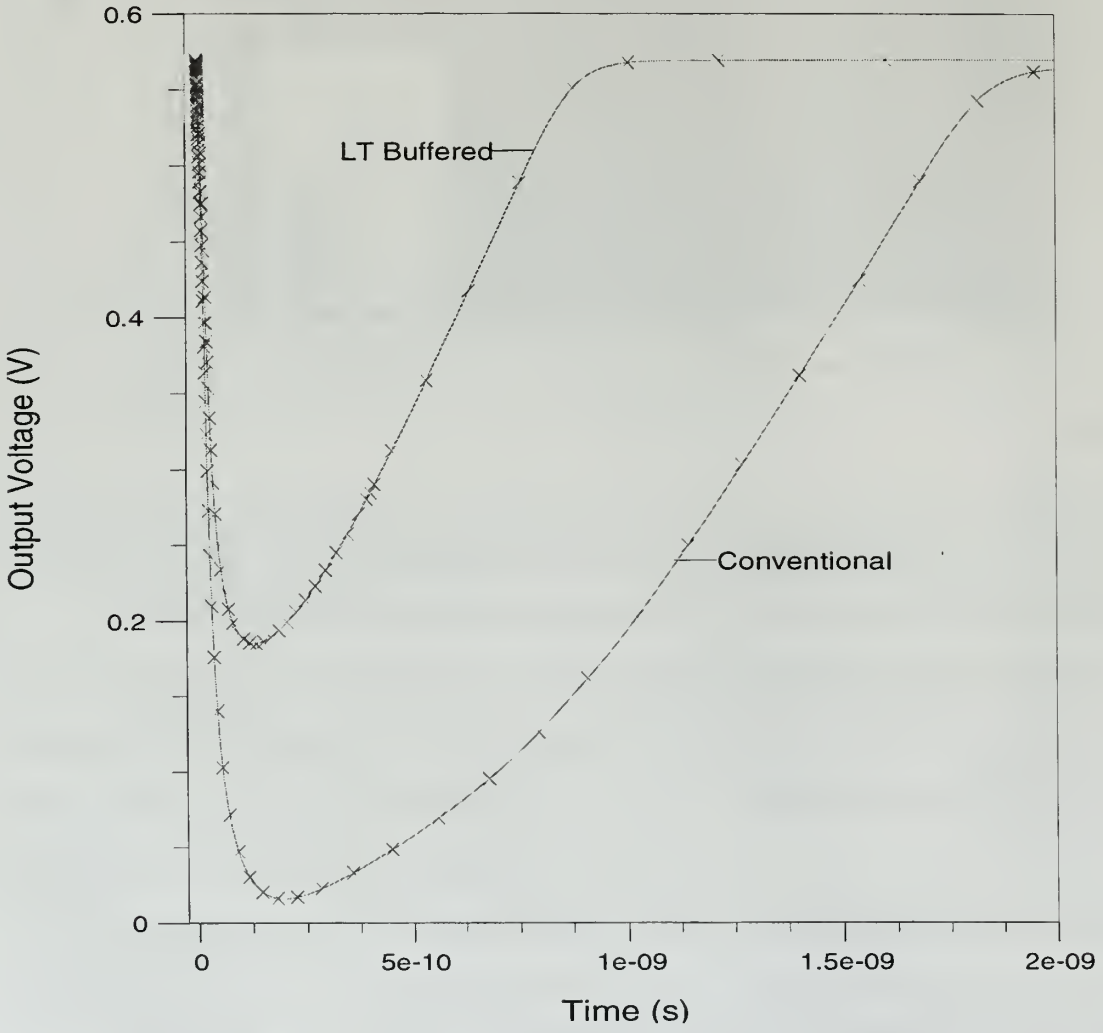

Figure 4.8 EFET drain voltage of an inverter SEU simulations, one with a conventional EFET and the other with LT GaAs Buffered EFET.

F. PULSE INTENSITY

Figures 4.9 and 4.10 shows how the output voltage waveform for simulations of various pulse intensities, and Table 4.1 shows the results in tabular form. These results show that the LT GaAs buffer shows a greater improvement over the conventional device for all intensities. The LT GaAs device also shows an improvement in recovery time.

EFET Type	Pulse Intensity	LET	Upset?	Between NMs	Time to Recover (ps)
Conventional	1 x 10^6 W/cm^2	0.08	NO	NO	N/A
Conventional	2 x 10^6 W/cm^2	0.16	YES	NO	367
Conventional	3 x 10^6 W/cm^2	0.25	YES	NO	706
Conventional	5 x 10^6 W/cm^2	0.42	YES	NO	1260
LT Buffer	1 x 10^6 W/cm^2	0.08	NO	NO	N/A
LT Buffer	3 x 10^6 W/cm^2	0.25	NO	YES	60.2
LT Buffer	5 x 10^6 W/cm^2	0.42	YES	NO	449
LT Buffer	7 x 10^6 W/cm^2	0.59	YES	NO	798

Table 4.1 Response of circuits to variations in the intensity of the SEU. (Between NMs means that the output voltage minimum was below the lower limit of the high noise margin, but above the upper limit of the low noise margin.)

In digital circuits, the voltage at the output of a gate is the most important value. It must be outside the noise margins of the gate being driven, or it is not valid. Designers need to know how long it takes a gate to produce a valid output once it senses a valid input. This is true for both synchronous and asynchronous circuits. When designing systems that are to be used in a radiation environment where they would be susceptible to SEUs, it is important for the designer to know the duration of an event. Designers can then design their redundant and fault-tolerant systems with a worst case scenario. Solid state and device designers can use these simulations to determine what charge collection mechanisms are prolonging the event and why. Using these results, improvements can be made and verified with further simulations. This can save a large amount of time. Simulations only take weeks to run, where a fabrication can take several months.

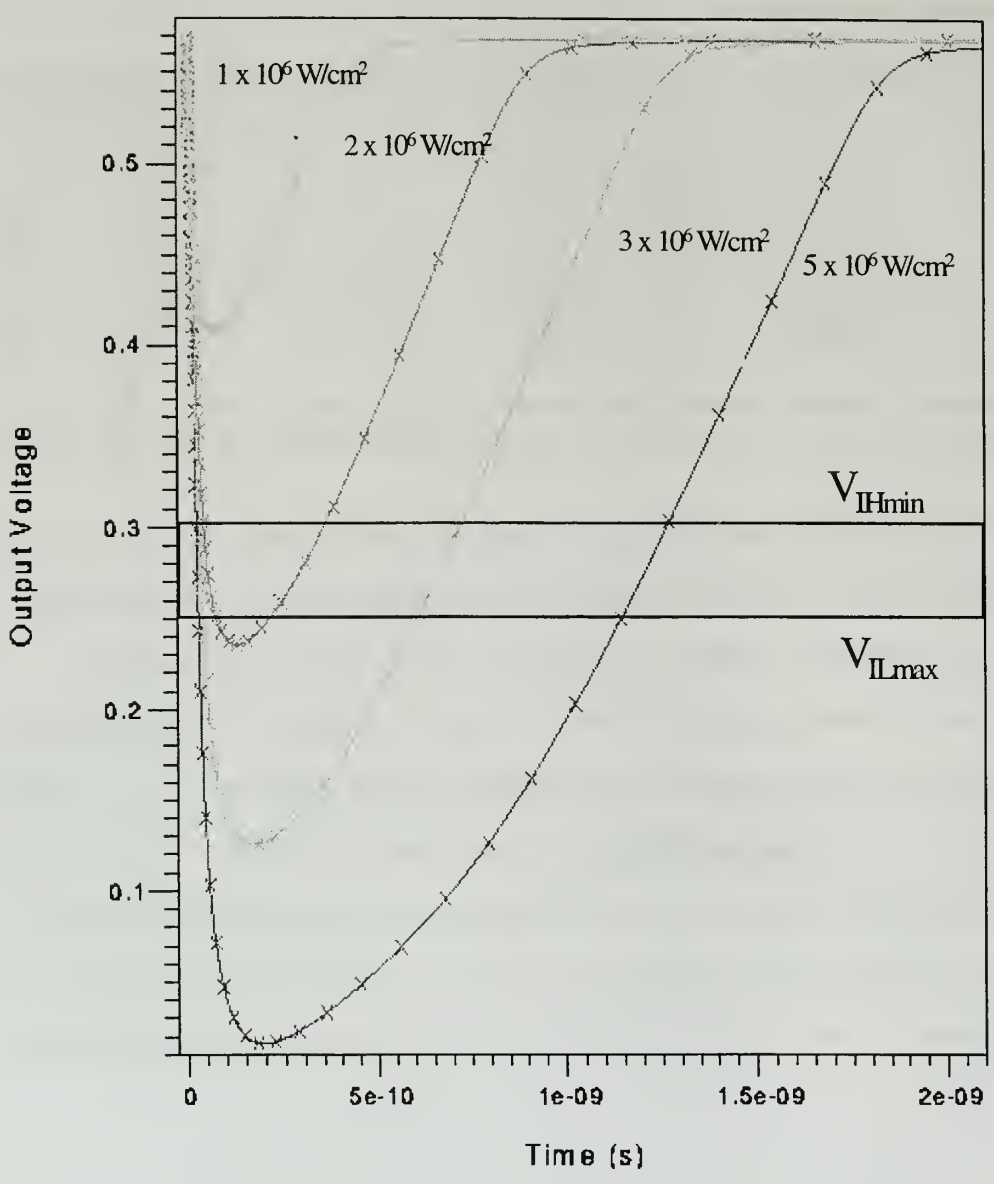

Figure 4.9 Response of inverter circuits with conventional EFETs to variations in the intensity of the SEU.

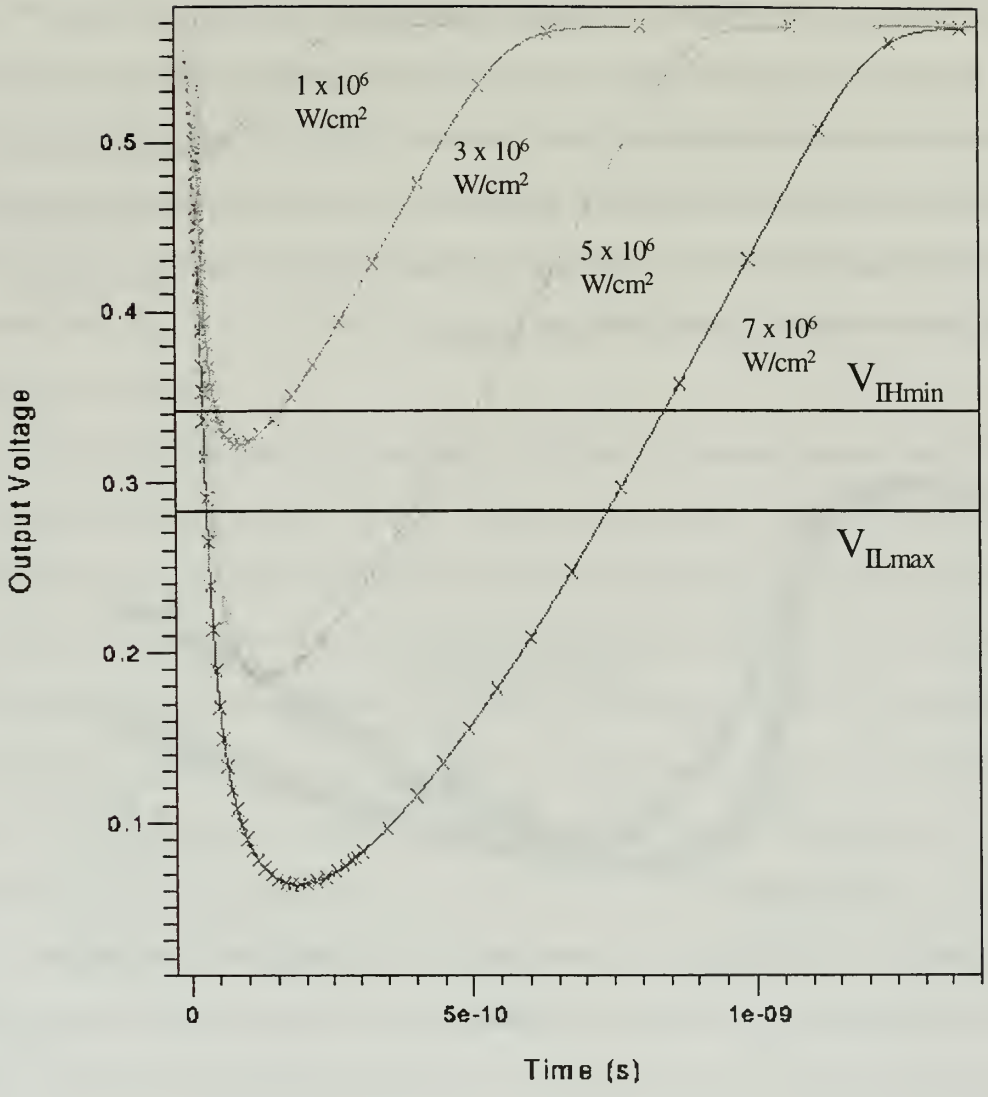

Figure 4.10 Response of inverter circuits with LT GaAs EFETs to variations in the intensity of the SEU.

G. COMPARISON TO EXPERIMENTAL MEASUREMENTS

The output voltage of an inverter during an SEU has been physically measured with picosecond resolution. [14] In conjunction with the University of Michigan's Center for Ultrafast Optics, Lieutenant Ezra Ledbetter, USN conducted SEU experiments with the same circuits that are simulated in this thesis. The event is induced with a laser, and the circuit output is measure with a resolution down to three picoseconds. Figure 4.11 shows how closely the simulation and experiment follow each other. These results show that the computer simulations are a viable method to accurately model the effects of an SEU in a GaAs MESFET. By testing theories via computer simulation first, valuable time in labs such as the one at the University of Michigan can be used as confirmation, rather than initial testing. Physical testing also requires costly, (and not so timely), wafer growth and fabrication.

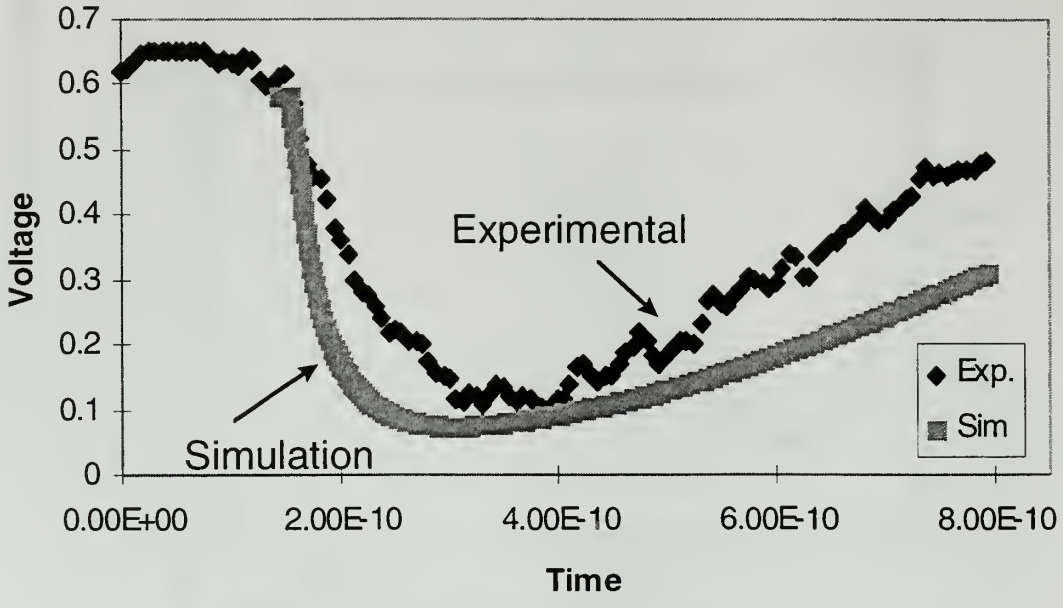

Figure 4.11 Output voltage of an inverter during an SEU. Experimental measurement and computer simulation results presented.

V. CONCLUSIONS

MIXEDMODE® is an effective tool for the 2-D computer modeling of SEUs and the analysis of the associated charge collection mechanisms. The results obtained from these simulations closely resemble those obtained in physical experiments, demonstrating the accuracy of these simulations. However, it is important to model the device being upset in a circuit to determine how the device interacts with other circuit devices during the event. Charge collection mechanisms in the device are the dominant factor effecting the performance of the circuit immediately following the SEU. The reaction of other devices in the circuit begin to dominate before the upset device has fully recovered. If the device is modeled discretely, then these 'tail-end' effects are given more credibility than they should because they no longer effect circuit performance.

LT GaAs buffers have shown considerable advantages in reducing soft error rates in GaAs ICs [4,5]. The properties of the buffer to act as an efficient structure to sink excess carriers by recombination has been shown in this work. The mechanisms to limit prompt charge (assisted with diffusion barriers) are very similar to those in silicon on insulator (SOI) technologies. Additionally, LT GaAs has advantages over SOI in reducing charge collection due to its high density of recombination centers. We have shown that excess charge above and below the buffer is sinked by recombination currents internal to the buffer. However, the buffer recombination rate can be compromised by diffusion barriers intended to confine arsenic to the buffer during MBE growth.

Manufacturing issues (growth temperatures, annealing techniques, structure design) are currently being investigated. The challenges in the Vitesse technology are greater due to the replacement of the bulk wafer by a MBE wafer and higher processing temperatures. Successful implementation of LT GaAs buffers will provide a very cost effective technique to harden GaAs implanted MESFET circuits against soft errors. Once the LT GaAs structure is optimized for both fabrication and charge collection, previous and future mask designs can utilize this hardening technique.

VI. FUTURE WORK

A. THREE-DIMENSIONAL MODELING

Once developed, three-dimensional models will improve the accuracy in two ways. The first is that the calculations in the device will add depth to our ability to see what is happening inside the device. The second is that the ion strike can be modeled closer to the physical dimensions of an ion. In the 2-D simulations, the ion strike is modeled with a plane of charge. While this is close enough to determine the reaction of the device, a more accurate simulation will provide more insight. It is expected that the effects due to prompt charge and the parasitic bipolar action will be diminished. The downfall of three-dimensional modeling is that is takes a large amount of computer time. Simulations that take one to two weeks with our present computers will at least double in execution time when done in 3-D. More powerful computers will be required for 3-D simulations. It may be possible to utilize this software on other Department of Defense computer resources.

B. INCREASED CIRCUIT COMPLEXITY

More complex circuit descriptions may provide greater insight to the device's interaction to the circuit during an SEU. Replacing the DFET, output load, and input with ATLAS® models in the current inverter configuration will increase the accuracy of the model and may provide useful insight. The performance of a more complex circuit, such as a memory cell, with the ATLAS® device as one of the devices should be explored to determine if the circuit effects become more dominant as the circuit becomes more complex. If several types of circuits are simulated and compared, an optimum utilization for the device may be determined (if one exists). It can be expected that there is a limit to the number of circuit configurations that can be explored and still provide useful data. As mentioned in the previous section, modeling these more complex circuits in three dimensions will provide the most accurate data.

C. VARIED PARAMETERS OF THE SEU

This thesis addressed the most sensitive SEU case; an ion strike between the drain and gate of the off enhancement device of an inverter that has zero volt input. By analyzing all the possibilities, the data collected will be used to fully characterize the SEU vulnerability of a device and to calculate both the overall and worst-case reliability of the device. There are several variations of SEU simulations that should be performed to determine their effects on the circuit:

1. Change positioning of the ion strike.
    a) Between gate and source.
    b) On each of the electrodes.
    c) From each of the sides of the device.
    d) From the bottom (substrate) of the device.
2. Change the incident angle of each strike.
3. Perform the various position and angle ion strikes on the DFET.

APPENDIX: EXAMPLE SILVACO INPUT CODE

```
#    DC bias point simulation of a Vitesse Inverter -
#       -Uses an Atlas model of a Vitesse Enhancement MESFET w/out LT GaAs Buffer
#       -Uses a MIXEDMODE mosfet as the active, depletion load
#       -A capacitor and diode in parallel model the gate of the next inverter.  (MIXEDMODE devices)
#       -Ideal voltage sources are used to supply both the input (Vin) and bias (Vcc) voltages.
#
#    This simulation ramps the bias voltage from zero to two volts in one-tenth of a volt steps.
#    The final solution from this simulation will be used as the initial starting point for all subsequent
#     simulations with this circuit.
#
#    INPUT File Name for the format file of the Atlas Device:     INITnolt1.str
#    OUTPUT File Names for initial guess starting positions:      noltMOS_I3
#                                                                 noltMOS_I3.cir
#
go atlas                                    # Starts the Atlas module
#
.begin                                      # Mixedmode Circuit description
#
vin   1   0   0                             # Input Voltage applied to the gate of the atlas device.
#
vcc   3   0   0.                            # DC bias voltage source
#
#
# Atlas model of a Vitesse EFET w/out LT GaAs buffer
aEFET 0=source 1=gate 2=drain infile=INITnolt1.str width=16.
#
```

```
#
mLOAD 3 2 2 2 MOS1  L=1.6u W=2.0u          # Mixedmode MOSFET as an active depletion load
#
# Output Load (Simulates the gate characteristic of the subsequent Vitesse inverter.)
dGATE  2 0 gs_junc  1                      # Simulates the gate-source junction
cGATE  2 0 50ff                            # Simulates the gate capacitance
#
#    End of Mixedmode circuit description
#
#
# Definition of the parameter for the Mixedmode models:
.model MOS1 nmos (kp=5e-5 vt0=-0.8)
.model gs_junc D (IS = 1e-14   RS = 1e-4   N   = 1   TT = 0   FC = 0.5   CJ0 = 0   MJ = 0.5   VJ = 0.65)
#
# Parameters and limits to be used in the mathematical analysis
.numeric        imaxdc = 20 \     # Maximum number of iterations during a DC solution
                imaxtr = 10 \     # Maximum number of iterations during a transient solution
                toldc = 1e-6 \    # Required tolerance during DC solutions
                toltr = 1e-6 \    # Required tolerance during DC solutions
                vmax = 2.5 \      # Maximum allowed voltage in the circuit
                vmin = 0.0 \      # Minimum allowed voltage in the circuit
                vchange= 1.0 \    # Maximum voltage change allowed between solutions
                dtmin = 1e-16 \   # Minimum time step allowed during transient solutions
                lte    = 1e-4 \   # Truncation Error
#


# Mixedmode Options:
```

```
.options        m2ln \          # Use Modified-Two-Level Newton Method to obtain a solution
#               noshift \       # Shifting of potential enabled because "noshift" is commented out
                relpot \        # Use relative convergence criteria for potentials
                print \         # Print circuit parameters to screen/output file
                write = 5 \     # Every fifth transient solution saved during saves
                tnom = 300 \    # Temperature for circuit calculations
                rv = 1e-4 \     # Resistance associated with voltage sources
                cnode = 0.0 \   #Capacitance between nodes and ground.
#
.dc vcc  0.0  2.0  0.1                  # Ramps the bias voltage from 0 to 2 Volts
#
.save outfile=noltMOS_I3                # Saves the final solution
#
.end                                    # End of Mixedmode simulation description
#
# Define physical models for Vitesse EFET atlas model
#
contact device=aEFET name=gate workfunction=4.87
contact device=aEFET name=drain
contact device=aEFET name=source
material taun0=1.e-9 taup0=1.e-9

models device=aEFET conmob fldmob srh bgn print evsatmod=1 hvsatmod=1 drift.diff all

options verbose ^normal ^quiet

output j.total e.field charge recomb \
```

```
^jx.total    ^ex.field     con.band    ^u.auger    \
^jy.total    ^ey.field     val.band    ^u.radiative \
j.electron   e.mobility    ^vectors    ^u.srh      \
^jx.electron ^e.temp       ^flowlines  ^band.param  \
^jy.electron ^e.velocity   ^impact     ^qfn        \
j.hole       ^ex.velocity  ^minset     ^qfp        \
^jx.hole     ^ey.velocity  ^photogen   ^qss        \
^jy.hole     h.mobility    ^opt.intens tot.doping  \
j.conduc     ^h.temp       ^ox.charge  ^traps      \
^jx.conduc   ^h.velocity   ^x.comp     ^devdeg     \
^jy.conduc   ^hx.velocity  ^y.comp                 \
j.disp       ^hy.velocity

#    DC Transfer Curve simulation of a Vitesse Inverter -
#      -Uses an Atlas model of a Vitesse Enhancement MESFET w/out LT GaAs Buffer
#      -Uses a MIXEDMODE mosfet as the active, depletion load
#      -A capacitor and diode in parallel model the gate of the next inverter.  (MIXEDMODE devices)
#      -Ideal voltage sources are used to supply both the input (Vin) and bias (Vcc) voltages.
#
#   This simulation ramps the input (gate) voltage from zero to one volt in one-tenth of a volt steps.
#   The final solution from this simulation will be used as the initial starting point for all subsequent
#    simulations with this circuit.
#
#   INPUT File Name for the format file of the Atlas Device:          INITnolt1.str
#                        for initial guess starting positions:        noltMOS_I3
#                                                                     noltMOS_I3.cir
#   OUTPUT File Names:  for structure file of final solution     DC_3
```

```
#                    for log file containing circuit data      DC_3.log
#
go atlas                                        # Starts the Atlas module
#
.begin                                          # Mixedmode Circuit description
#
vin   1   0   0                                 # Input Voltage applied to the gate of the atlas device.
#
vcc   3   0   2.                                # DC bias voltage source
#
#
# Atlas model of a Vitesse EFET w/out LT GaAs buffer
aEFET 0=source 1=gate 2=drain infile=INITnolt1.str width=16.
#
#
mLOAD 3 2 2 2 MOS1  L=1.6u W=2.0u               # Mixedmode MOSFET as an active depletion load
#
# Output Load (Simulates the gate characteristic of the subsequent Vitesse inverter.)
dGATE  2 0 gs_junc  1                           # Simulates the gate-source junction
cGATE  2 0 50ff                                 # Simulates the gate capacitance
#
#    End of Mixedmode circuit description
#
#
# Definition of the parameter for the Mixedmode models:
.model MOS1 nmos (kp=5e-5 vt0=-0.8)
.model gs_junc D (IS = 1e-14   RS = 1e-4   N   = 1   TT = 0   FC = 0.5   CJ0 = 0   MJ = 0.5   VJ = 0.65)
```

```
#
# Parameters and limits to be used in the mathematical analysis
.numeric        imaxdc = 20 \     # Maximum number of iterations during a DC solution
                imaxtr = 10 \     # Maximum number of iterations during a transient solution
                toldc = 1e-6 \    # Required tolerance during DC solutions
                toltr = 1e-6 \    # Required tolerance during DC solutions
                vmax = 2.5 \      # Maximum allowed voltage in the circuit
                vmin = 0.0 \      # Minimum allowed voltage in the circuit
                vchange= 1.0 \    # Maximum voltage change allowed between solutions
                dtmin = 1e-16 \   # Minimum time step allowed during transient solutions
                lte   = 1e-4 \    # Truncation Error
#

# Mixedmode Options:
.options        fulln \           # Use Full Newton Method to obtain a solution
#               noshift \         # Shifting of potential enabled because "noshift" is commented out
                relpot \          # Use relative convergence criteria for potentials
                print \           # Print circuit parameters to screen/output file
                write = 5 \       # Every fifth transient solution saved during saves
                tnom = 300 \      # Temperature for circuit calculations
                rv = 1e-4 \       # Resistance associated with voltage sources
                cnode = 0.0 \     #Capacitance between nodes and ground.
#
.nodeset V(1)=0.0  V(2)=0.5699  V(3)=2.0        # Initial guess of circuit voltages
##
.load infile=noltMOS_I3                         # Solution from DC bias calculation
.log outfile=DC_3                               # Log circuit data throughout simulation
```

```
.dc vin 0. 1. 0.01                    # Ramp input voltage from 0 to 1 Volt
#
.save outfile=DC_3.str                # Saves the final solution
#
.end                                  # End of Mixedmode simulation description
#
# Define physical models for Vitesse EFET atlas model
#
contact device=aEFET name=gate workfunction=4.87
contact device=aEFET name=drain aluminum
contact device=aEFET name=source aluminum
material taun0=1.e-9 taup0=1.e-9

models device=aEFET conmob fldmob srh bgn print evsatmod=1 hvsatmod=1 drift.diff all

options verbose ^normal ^quiet

output j.total     e.field     charge     recomb    \
     ^jx.total    ^ex.field    con.band   ^u.auger   \
     ^jy.total    ^ey.field    val.band   ^u.radiative \
      j.electron   e.mobility   ^vectors   ^u.srh     \
     ^jx.electron ^e.temp      ^flowlines  ^band.param \
     ^jy.electron ^e.velocity  ^impact     ^qfn       \
      j.hole      ^ex.velocity ^minset     ^qfp       \
     ^jx.hole     ^ey.velocity ^photogen   ^qss       \
     ^jy.hole     h.mobility   ^opt.intens tot.doping \
      j.conduc    ^h.temp      ^ox.charge  ^traps     \
```

```
    ^jx.conduc   ^h.velocity   ^x.comp     ^devdeg    \
    ^jy.conduc   ^hx.velocity  ^y.comp              \
    j.disp     ^hy.velocity

go atlas

#    DC Transfer Curve simulation of a Vitesse Inverter -
#      -Uses an Atlas model of a Vitesse Enhancement MESFET w/out LT GaAs Buffer
#      -Uses a MIXEDMODE mosfet as the active, depletion load
#      -A capacitor and diode in parallel model the gate of the next inverter.  (MIXEDMODE devices)
#      -Ideal voltage sources are used to supply both the input (Vin) and bias (Vcc) voltages.
#
#   This simulation ramps the input (gate) voltage from zero to one volt in one-tenth of a volt steps.
#   The final solution from this simulation will be used as the initial starting point for all subsequent
#    simulations with this circuit.
#
#   INPUT File Name for the format file of the Atlas Device:          INITnolt1.str
#                        for initial guess starting positions:        noltMOS_I3
#                                                                     noltMOS_I3.cir
#   OUTPUT File Names:  for structure file of final solution     DC_3
#                            for log file containing circuit data     DC_3.log
#
go atlas                                        # Starts the Atlas module
#
.begin                                          # Mixedmode Circuit description
#
vin  1  0  0                                    # Input Voltage applied to the gate of the atlas device.
```

```
#
vcc  3  0  2.                          # DC bias voltage source
#
# Optical Pulse incident between the gate and the drain to induce the single event upset.
# Name  Terminals   Type   Intensity    Delay   Rise Time   Fall Time   Pulse Width     Period
Oion      1   0       pulse    0  5.0e6   1.90ps    .25ps       .25ps          .5ps         100ns
#
#
# Atlas model of a Vitesse EFET w/out LT GaAs buffer
aEFET 0=source 1=gate 2=drain infile=INITnolt1.str width=16.
#
#
mLOAD 3 2 2 2 MOS1  L=1.6u W=2.0u          # Mixedmode MOSFET as an active depletion load
#
# Output Load (Simulates the gate characteristic of the subsequent Vitesse inverter.)
dGATE  2 0 gs_junc  1                      # Simulates the gate-source junction
cGATE  2 0 50ff                            # Simulates the gate capacitance
#
#    End of Mixedmode circuit description
#
#
#  Definition of the parameter for the Mixedmode models:
.model MOS1 nmos (kp=5e-5 vt0=-0.8)
.model gs_junc D (IS = 1e-14   RS = 1e-4   N   = 1   TT = 0   FC = 0.5   CJ0 = 0   MJ = 0.5   VJ = 0.65)
#
#  Parameters and limits to be used in the mathematical analysis
.numeric          imaxdc = 20 \     # Maximum number of iterations during a DC solution
```

```
                imaxtr = 10 \      # Maximum number of iterations during a transient solution
                toldc = 1e-6 \     # Required tolerance during DC solutions
                toltr = 1e-6 \     # Required tolerance during DC solutions
                vmax = 2.5 \       # Maximum allowed voltage in the circuit
                vmin = 0.0 \       # Minimum allowed voltage in the circuit
                vchange= 1.0 \     # Maximum voltage change allowed between solutions
                dtmin = 1e-16 \    # Minimum time step allowed during transient solutions
                lte    = 1e-4 \    # Truncation Error
#

# Mixedmode Options:
.options        fulln \            # Use Full Newton Method to obtain a solution
#               noshift \          # Shifting of potential enabled because "noshift" is commented out
                relpot \           # Use relative convergence criteria for potentials
                print \            # Print circuit parameters to screen/output file
                write = 5 \        # Every fifth transient solution saved during saves
                tnom = 300 \       # Temperature for circuit calculations
                rv = 1e-4 \        # Resistance associated with voltage sources
                cnode = 0.0 \      #Capacitance between nodes and ground.
#
.nodeset V(1)=0.0  V(2)=0.5699  V(3)=2.0        # Initial guess of circuit voltages
##
.load infile=noltMOS_I3                         # Solution from DC bias calculation
.log outfile=SEU_3                              # Log circuit data throughout simulation
#
.tran      .5ps      2.5ns                      #Perform transient solution for 2.5 nanoseconds
                                                #starting with .5 picosecond steps.
```

```
#
# Create atlas structure files for each step of simulation and a final solution
.save outfile=SEU_4_final master=SEU_4
#
.end                                    # End of Mixedmode simulation description
#
#  Define physical models for Vitesse EFET atlas model
#
contact device=aEFET name=gate workfunction=4.87
contact device=aEFET name=drain
contact device=aEFET name=source
material taun0=1.e-9 taup0=1.e-9 copt=1.5e-10

models device=aEFET  conmob   fldmob  srh  bgn   print  evsatmod=1  hvsatmod=1 drift.diff  all  optr

options  ^verbose  ^normal  quiet

output  j.total     e.field      charge      recomb     \
      ^jx.total    ^ex.field     con.band    ^u.auger    \
      ^jy.total    ^ey.field     val.band    ^u.radiative \
       j.electron   e.mobility   ^vectors    ^u.srh      \
      ^jx.electron  ^e.temp      ^flowlines  ^band.param  \
      ^jy.electron  ^e.velocity  ^impact     ^qfn        \
       j.hole      ^ex.velocity  ^minset     ^qfp        \
      ^jx.hole     ^ey.velocity  ^photogen   ^qss        \
      ^jy.hole     h.mobility    ^opt.intens  tot.doping  \
       j.conduc    ^h.temp       ^ox.charge   ^traps      \
```

```
^jx.conduc   ^h.velocity   ^x.comp     ^devdeg    \
^jy.conduc   ^hx.velocity  ^y.comp              \
 j.disp      ^hy.velocity
```

Defines the model for the optical beam that inserts charge equivelent to an ion

```
beam  angle=90 device=aEFET max.window=.125 min.window=-.125 number=1 x.origin=3 y.origin=-.06
```

quit	Closes the Atlas Module

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